REMARKS

Summary of the Amendment

Upon entry of the Applicants' amendment, claims 14 – 20 will have been canceled without prejudice or disclaimer, and new claims 21 and 22 will have been entered for consideration by the Examiner. Further, Applicants have expressly reserved the right refile the subject matter of canceled claims 13 – 20 in one or more divisional applications. Therefore, claims 1 – 13, 21, and 22 are currently pending.

Summary of the Official Action

In the instant Office Action, the Examiner has rejected claims 1 – 13 over the art of record. By the present amendment and remarks, Applicants submit that the rejections have been overcome, and respectfully request reconsideration of the outstanding Office Action and allowance of the present application.

Traversal of Rejection Under 35 U.S.C. § 102(e)

1. Independent claim 1+

Applicants traverse the rejection of claims 1 – 3, 5, 8, and 9 under 35 U.S.C. § 102(e) as being anticipated by ACHUTHAN et al. (U.S. Patent No. 7,125,776) [hereinafter "ACHUTHAN"]. The Examiner, referring to Figs. 1 – 5, asserts ACHUTHAN shows each and every feature of the above-identified claims. Applicants traverse the Examiner's assertions.

Applicants' independent claim 1 recites, *inter alia*, a silicon on insulator layer having *a plurality of channels*, a silicon oxide insulation layer *adjacent* the silicon on insulator layer, and a dielectric layer *adjacent* the silicon oxide insulation layer, wherein *at least one channel* has a gate configuration that is *different than the remaining channels*. Applicants submit ACHUTHAN fails to disclose at least the above-noted feature of the invention.

With reference to ACHUTHAN's figure 3, Applicants note, contrary to the Examiner's assertions layer 110 is not a silicon on insulator layer, nor is there any disclosure of a plurality of channels associated with this layer. Further, ACHUTHAN fails to disclose that silicon layer 130 is a dielectric, as asserted by the Examiner.

Applicants direct the Examiner's attention to col. 2, lines 62 – 65, which discloses ACHUTHAN's device includes a "*silicon on insulator (SOI) structure that includes* a silicon substrate 110, a buried oxide layer 120 and a silicon layer 130 formed on the buried oxide layer 120." [emphasis added]. Thus, in contrast to the Examiner's assertions, ACHUTHAN discloses the *combination* of layers 110, 120, and 130 form a silicon on insulator structure, while layer 110 individually is a "silicon" substrate. Further, as silicon is a semiconductor material, Applicants submit there is no arguable disclosure of silicon layer 130 being a dielectric layer, as recited in Applicants' claims.

Thus, Applicants submit the Examiner's rejection of independent claim 1 is based upon a mischaracterization or misinterpretation of the disclosure of ACHUTHAN, and that ACHUTHAN fails to disclose each and every recited element of at least independent claim 1.

In contrast to Applicants' independent claim 1, fin 210 of ACHUTHAN is only disclosed as being composed of a stacked arrangement of silicon layer 130 and a dielectric 140, with sacrificial dielectric layer 310 grown on fin 210. However, ACHUTHAN fails to disclose a fin having a silicon oxide insulation layer, as recited in at least Applicants' independent claim 1.

Finally, Applicants note the Examiner has not identified a plurality of channels, nor has the Examiner identified any specific disclosure in ACHUTHAN that even arguably suggests the transistor of ACHUTHAN includes at least one channel with a gate configuration that is different from remaining channels. Thus, for this additional reasoning, Applicants submit ACHUTHAN

fails to show each and every recited elements of Applicants' claims.

As the applied art fails to disclose each and every recited element of at least independent claim 1, Applicants submit the Examiner has failed to establish an adequate evidentiary basis to support a rejection of anticipation under 35 U.S.C. § 102(e), such that the pending rejection is improper and should be withdrawn.

Further, Applicants submit that claims 2, 3, 5, 8, and 9 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular, Applicant submits that ACHUTHAN fails to anticipate the invention recited in claims 2, 3, 5, 8, and 9.

Accordingly, Applicants request the Examiner reconsider and withdraw the rejections of claim 1 – 3, 5, 8, and 9and indicate these claims are allowable in the next official communication.

2. Independent claim 10+

Applicants traverse the rejection of claims 10 – 13 under 35 U.S.C. § 102(e) as being anticipated by ACHUTHAN. The Examiner again refers to Figs. 1 – 5 in asserting ACHUTHAN shows each and every feature of the above-identified claims. Applicants traverse the Examiner's assertions.

Applicants' independent claim 10 recites, *inter alia*, a stack comprising a silicon on insulator layer, *a silicon oxide insulation layer on the silicon* on insulator layer, *a dielectric layer on the silicon oxide insulation layer*, wherein the dielectric layer is a high-k dielectric material, and *a protection layer on the dielectric layer*. Applicants submit ACHUTHAN fails to disclose at least the above-noted feature of the invention.

As discussed in detail above, ACHUTHAN's Figure 3 does not disclose the subject

matter alleged by the Examiner in the pending Office Action. That is, contrary to the Examiner's assertions, there is no disclosure that layer 110 of ACHUTHAN is a silicon on insulator layer, nor is there any disclosure that silicon layer 130 is a dielectric layer, and in particular a high-k dielectric material, as recited in Applicants' claims.

Applicants again direct the Examiner's attention to col. 2, lines 62 – 65, which discloses ACHUTHAN's device includes a "*silicon on insulator (SOI) structure that includes* a silicon substrate 110, a buried oxide layer 120 and a silicon layer 130 formed on the buried oxide layer 120." [emphasis added]. Thus, in contrast to the Examiner's assertions, ACHUTHAN discloses the *combination* of layers 110, 120, and 130 form a silicon on insulator structure, while layer 110 individually is a "silicon" substrate. Further, as silicon is a semiconductor material, Applicants submit there is not arguable disclosure of silicon layer 130 being a dielectric layer, as asserted by the Examiner.

Thus, Applicants submit the Examiner's rejection of independent claim 10, like the rejection of independent claim 1, is based upon a mischaracterization or misinterpretation of the disclosure of ACHUTHAN, and that ACHUTHAN fails to disclose each and every recited element of at least independent claim 10.

While Applicants' independent claim 10 recites, *inter alia*, a "stack comprising" the above-noted recited elements, fin 210 in ACHUTHAN is only disclosed as being composed of a stacked arrangement of silicon layer 130 and a dielectric 140, with sacrificial dielectric layer 310 grown on fin 210. Thus, ACHUTHAN fails to disclose a fin having a silicon oxide insulation layer and fails to disclose a high-k dielectric material, as recited in at least Applicants' independent claim 10.

As the applied art fails to disclose each and every recited element of at least independent

claim 1, Applicants submit the Examiner has failed to establish an adequate evidentiary basis to support a rejection of anticipation under 35 U.S.C. § 102(e), such that the pending rejection is improper and should be withdrawn.

Further, Applicants submit that claims 11 – 13 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular, Applicant submits that ACHUTHAN fails to anticipate the invention recited in claims 11 – 13.

Accordingly, Applicants request the Examiner reconsider and withdraw the rejections of claim 10 – 13 indicate these claims are allowable in the next official communication.

Traversal of Rejection Under 35 U.S.C. § 103(a)

Applicants traverse the rejection of claims 4, 6, 7, 11, and 12 under 35 U.S.C. § 103(a) as being unpatentable over ACHUTHAN. While acknowledging ACHUTHAN fails to show the gate dielectric of the remaining channels is a material comprising silicon dioxide, nitride dioxide, and silicon oxide that has undergone a plasma nitridation process, or the cover layer is metal or thin polysilicon, the Examiner asserts it would have been obvious to modify ACHUTHAN to include these features. Applicants traverse the Examiner's assertions.

As Applicants have noted in responses to previous Office Actions, Examiner's assertion regarding the phrase "silicon oxide that has undergone a plasma nitridation process" is contrary to Applicants' disclosure. That is, the above-noted phrase is not a product by process limitation, but a recitation of a specific material utilized in the structure of the invention. In this regard, the claim at issue does not recite any process steps, such that the Examiner's assertions regarding a product by process limitation is inaccurate and should be withdrawn.

Moreover, while objecting to the recitation as product by process, the Examiner has not

identified any of the materials recited in Applicants' claim 4 that would have been rendered obvious by ACHUTHAN. Further, Applicants note the Examiner has not identified a plurality of channels disclosed by ACHUTHAN, nor has the Examiner identified any disclosure by ACHUTHAN of various channels being formed of different gate dielectric materials. Thus, Applicants submit the Examiner has not provided a *prima facie* case of obviousness under 35 U.S.C. § 103(a).

With regard to the protection layer being formed of metal or polysilicon, the Examiner has merely asserted it would have been obvious to modify ACHUTHAN to use such materials since it is known to select a material on the basis of its suitability for a desired application, which the Examiner asserts is for making a mask or protecting layers during etching or patterning. However, the Examiner has not identified any disclosure in ACHUTHAN of a layer that is a mask or is arranged to protect layers during etching or patterning, or that it would have been obvious to form such a layer from metal or a polysilicon, as asserted by the Examiner. Should the Examiner want to maintain this rejection in a next Official Action, Applicants request the Examiner identify the portions of ACHUTHAN's disclosure relied upon in rejecting the claims so Applicants can better the address the Examiner's conclusory arguments of obviousness.

Further, Applicants submit that claims 4, 6, 7, 11, and 12 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular, Applicant submits that ACHUTHAN fails to anticipate the invention recited in claims 4, 6, 7, 11, and 12.

Accordingly, Applicants request the Examiner reconsider and withdraw the rejections of claim 4, 6, 7, 11, and 12 and indicate these claims are allowable in the next official communication.

Newly Submitted Claims are Allowable

Applicants submit that newly presented claims 21 and 22 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular, Applicant submits that ACHUTHAN fails to anticipate or render unpatentable the invention recited in claims 21 and 22.

In this regard, new claims 21 and 22, which depend from independent claims 1 and 10, respectively, recite, *inter alia*, that the stack is arranged such that the silicon on insulator layer, the silicon oxide insulation layer, and the dielectric layer are located one on top of the other. Applicants note ACHUTHAN, whether considered alone or in any proper combination with any other document of record, fails to render unpatentable the combination of features recited in at least new claims 21 and 22.

Accordingly, Applicants request consideration and allowance of new claims 21 and 22.

Application is Allowable

Thus, Applicants respectfully submit that each and every pending claim of the present invention meets the requirements for patentability under 35 U.S.C. §§ 102 and 103, and respectfully request the Examiner to indicate allowance of each and every pending claim of the present invention.

Authorization to Charge Deposit Account

The undersigned authorizes the charging of any necessary fees, including any extensions of time fees required to place the application in condition for allowance by Examiner's Amendment, to Deposit Account No. 09 – 0458 in order to maintain pendency of this application.

CONCLUSION

In view of the foregoing, it is submitted that none of the references of record, either taken alone or in any proper combination thereof, anticipate or render obvious the Applicants' invention, as recited in each of claims 1 – 13, 21, and 22. The applied references of record have been discussed and distinguished, while significant claimed features of the present invention have been pointed out.

Accordingly, reconsideration of the outstanding Office Action and allowance of the present application and all the claims therein are respectfully requested and now believed to be appropriate.

Respectfully submitted,
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